Electronic Version
Stylesheet Version v1.1.1

INPUT BUFFER WITH HYSTERESIS OPTION

Abstract

The invention provides a high-speed buffer that may used at the input of an integrated circuit, such as an input buffer. This buffer may be configured for use as a standard buffer with a single switching threshold, such as a TTL-to-CMOS buffer, or used as a Schmitt trigger with hysteresis, which as at least two switching thresholds. The integrated circuit may be a programmable logic device (PLD) or field programmable gate array (FPGA), but in other embodiments, the integrated circuit may be other types of devices such a microprocessors, ASICs, or memories.